Dual Loop PLDRO

Description

The PLDRO (Phase Locked Dielectric Resonator Oscillator) provides the ultra-low phase noise and an excellent frequency stability when it is phase-locked to a clean and stable crystal reference signal. The PLDRO provides ideal signal for commercial and military systems that require ultra-low phase noise, low spurious, and high frequency stability.

Our PLDRO series are available in four series products: Single Loop PLDRO, Dual Loop PLDRO, Variable Frequency PLDRO, and Fractional-N PLDRO.

The Dual Loop PLDRO is a phase locked dielectric resonator oscillator whose output frequency is generated by a dual phase locked loop. This PLDRO series provides an output frequency whose phase is locked to an integer or fractional multiple of the external reference using PLCRO (Phase Locked Coaxial Resonator Oscillator) and frequency divider.

Features

- Integer or Fractional Multiple of the External Reference
- Ultra Low Phase Noise
- Low Spurious
- Phase-Locked Alarm
- Low Current Consumption
- Compact Housing
- Rugged Construction

Options

- Output Power: 17 dBm (typ.)
- Supply Voltage: 6 VDC
- Operating Temperature: -20 ℃ to 70 ℃/-40 ℃ to 70 ℃
- Field Replaceable SMA-Jack
- Laser Marking

Applications

- Radar Systems
- VSAT/Satellite Communication Systems
- Test Equipment
- Microwave Transmitters & Receivers
- Cable TV Links (CATV)
- LMDS
- Missile Guidance
- Local Area Networks (LAN)

Specifications

Parameters		Specifications			
Output Frequency		5 GHz to 28 GHz			
Output Power		15 dBm (typ.)			
Phase Noise (dBc/Hz)	Frequency / Offset	6 GHz	10 GHz	13 GHz	26 GHz
	100 Hz	-92	-87	-84	-78
	1 KHz	-112	-110	-106	-100
	10 KHz	-117	-113	-111	-105
	100 KHz	-120	-114	-112	-106
	1 MHz	-136	-130	-125	-122
External Reference	Frequency	10 MHz to 100 MHz			
	Input Power	0 ± 2 dBm			
Harmonics		-30 dBc (typ.), -20 dBc (max.)			
Sub-harmonics (N*Fout/2, N odd)		-25 dBc (typ.), -15 dBc (max.)			
Frequency Stability		Same as the Reference			
Spurious		-80 dBc (typ.), -70 dBc (max.)			
Pulling (3:1 VSWR) (max.)		Will not break lock			
Output Impedance		50 Ω			
Supply Voltage		12 ± 0.5 VDC			
Current Consumption		Consult Factory			
Connectors	RF Output (RF OUT)	SMA-Jack			
	External Reference Input (REF IN)	SMA-Jack			
	Supply Voltage (Vin)	EMI Feed-thru			
	Phase Voltage (Vp)	EMI Feed-thru			
	Phase Lock-Detect (LD) **Note 1**	EMI Feed-thru			
	GND	Turret Thread Mount Terminal			
Housing Size (W x L x H)		2.25"[57.15] x 2.25"[57.15] x 1.06"[27]			
Environmental Conditions	Operating Temperature	0 °C to 60 °C			
	Storage Temperature	-20 °C to 70 °C			

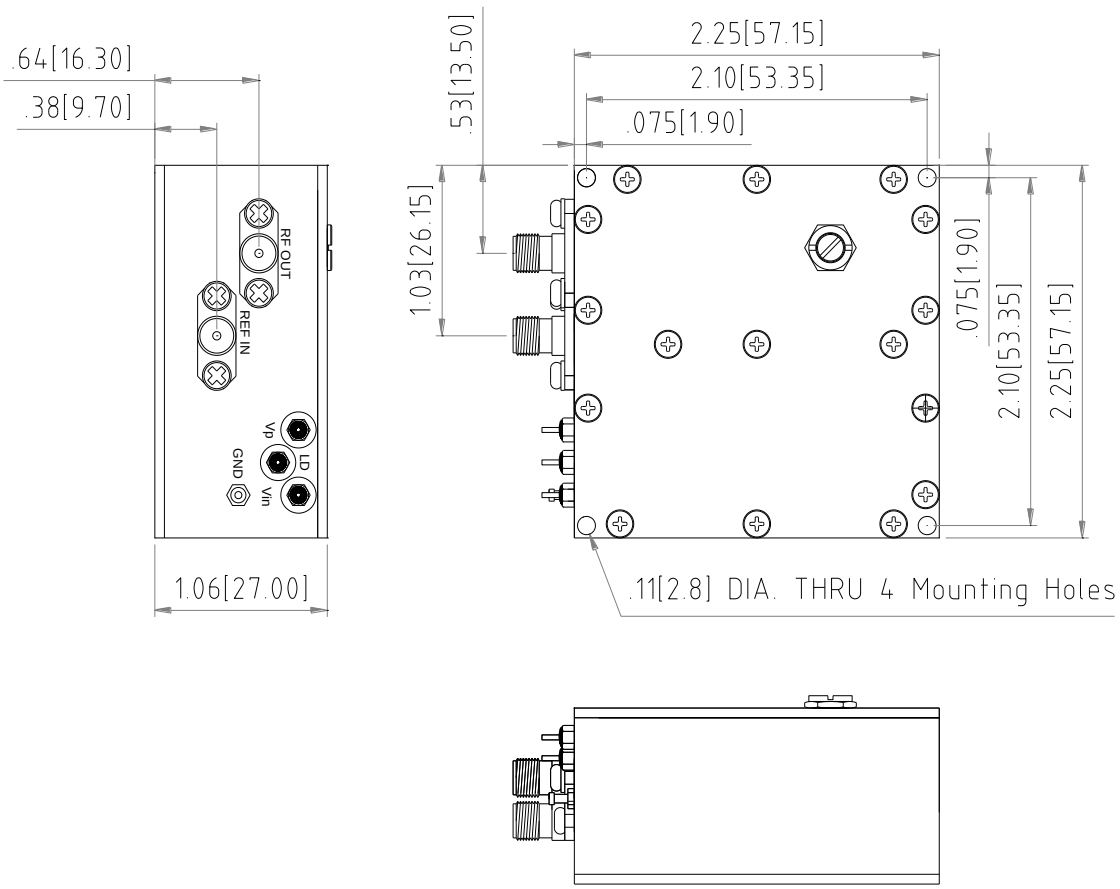
These specifications are subject to change without notice. Please contact the factory for the latest specifications.

Note 1 Phase Lock-Detect (LD)

- 3.3 V when phase locked
- 0 V when phase unlocked

Outline Drawing

Dimensions shown in brackets [ ] are in millimeters.



Dual Bed Housing

Ordering Information

wPLDRO-Rxxxx-y…y-Pzz-aa

- w: Product Categories
  - . S (Single Loop PLDRO)
  - . D (Dual Loop PLDRO)
  - . F (Fractional-N PLDRO)
- xxxx: Reference Frequencies (MHz)
  - . Ixxx: Internal, xxxMHz
  - . Exxx: External, xxxMHz
- y…y: Output Frequency (MHz)
- zz: Output Power (dBm)
- aa: Housing types
  - . SB (Single Bed Housing)
  - . DB (Dual Bed Housing)
  - . HS (Hermetically Sealed Housing)
  - . NP (Number of Ports)

Examples

DPLDRO-RE10-7742.5-P15-DB

. Product Category: Dual Loop PLDRO
. Reference Frequency: External, 10 MHz
. Output Frequency: 7,742.5 MHz
. Output power: 15 dBm
. Dual Bed Housing

DPLDRO-RE10-13125-P17-DB

. Product Category: Dual Loop PLDRO
. Reference Frequency: External, 10 MHz
. Output Frequency: 13,125 MHz
. Output power: 17 dBm
. Dual Bed Housing

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